EE Times:

Backplane design moves to center stage

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Switched serial interconnects have placed substantial performance demands on backplane design. The open-specification organizations VMEbus International Trade Association (VITA) and PCI Industrial Computing Manufacturers Group (PICMG) are offering new higher-speed backplane architectures; they plan to handle faster applications by using switched-fabric backplane technologies. To meet the challenging design requirements of 3.125- and 6.25-Gbit/second signaling and beyond, backplane designers will have to adopt new design methodologies and choose between new materials and printed-circuit-board fabrication techniques.

The main VITA effort, VXS-for VMEbus switched serial standard (VITA 41, part of the VME Renaissance)-is a Motorola-led initiative. The VXS design starts with a standard VME64x backplane design and implements a high-speed fabric by replacing the existing P0 connector with a new high-speed Multi-Gig seven-row connector and adding hub slots fully populated with the new connector. The PICMG effort is the Advanced Telecommunications Computing Architecture, or AdvancedTCA (PICMG 3.0), which is a new form factor and specification led by Intel and Lucent.

It is completely new and uses the high-speed ZD connector in a new 8U x 280-mm form factor, forgoing any backward compatibility with PICMG's popular CompactPCI. VXS and AdvancedTCA both support Ethernet, Infiniband, StarFabric, RapidIO and PCI Express and challenge engineers to find ingenious ways to maintain signal quality at a reasonable cost despite the negative influences of higher layer counts, greater signal densities and complex signal interactions. Some believe that the challenges met today at 3.125 and 6.25 Gbits/s will re-emerge as copper signaling moves toward 15 Gbits/s and possibly beyond.

The AdvancedTCA specification allows a variety of architectural implementations. An ingenious channel mapping allows a standard AdvancedTCA switch card to support any configuration. For instance, a dual-star (redundant hub slots running the fabric) implementation could be done with cards at either end of the

subrack, adjacent in Slots 1 and 2, or in the middle of the backplane. However, placing the hub slots in the center of the backplane reduces the maximum trace length by half. The result is a big improvement in signal quality because the losses due to dielectric and skin effect will be nearly halved. Further, placing the hub slots in the middle simplifies connections, allowing the layer count to drop from 18 to only 12 layers. This not only saves cost, but at 3.2 mm the thinner board has shorter via stubs-and stubs are one of the most significant loss contributors at gigabit data rates.

In a TDR profile of a stub for a trace situated in the first signal layer, the minimum differential impedance for this layer just below the connector was only 85 ohms and measurements indicated that the differential impedance the signal sees is 102 ohms. This optimized performance (within plus/minus 2 percent) is the result of careful trace design, laminate choice and manufacturing control. Tests using passive and active cards with real drivers operating at 3.125 Gbits/s validated the measurements. The measured eye opening of 509 mV leaves plenty of margin as these drivers only require a minimum opening of 200 mV. In a live system, performance may be better because the negative effects of the surface-mount-assembly contacts and cables would be eliminated. Measurements and tests both indicate that FR-4 can support speeds of over 5 Gbits/s with the AdvancedTCA layout.

But not all layouts are as generous; the new VXS architecture presented a substantially different challenge-remaining backward compatible within the existing VME64x backplane layout constraints.

VXS backplane

For VXS the new MultiGig RT P0 connector and hub slots carry the high-speed switch fabrics while the P1 and P2 connectors will support legacy VME64x cards. This design maintains full backward compatibility while adding high-speed serial-fabric connectivity. VITA 41 designers will have the flexibility of using the P2 connector in a payload slot for the parallel VME64x legacy cards or the P0 connector in the same payload slot for an Infiniband or RapidIO fabric connection. In the future, StarFabric and PCI Express may also be supported.

The existing 2-mm HM P0 connector would not support well any speeds over 1 Gbit/s; the new VXS design uses a seven-row MultiGig RT connector to handle speeds of up to 10 Gbits/s. However, accomplishing the dense routing on a 0.8-inch pitch with signals at 3.125 Gbits/s or higher requires some creativity. Even a midsize 12-slot dual-star VXS backplane configuration forces the designer to make some difficult choices.

Such a backplane requires as many as 18 layers. Avoiding undesirable stubs for upper-layer backplane traces presents two possible options. One choice would be to have these worst-case vias back-drilled, a costly fabrication process that removes the unused portion of the plated via structure below the layer at which the signal is terminated. The other choice is to minimize the length of via stubs by picking a laminate with a lower dielectric constant. This allows the 100-ohm differential impedance to be achieved

with thinner pc-board layers.

A lower dielectric constant (Er) is not the only characteristic that makes higher-performance board materials attractive. Materials such as Nelco 4000-13SI, Rogers 4350 and Matsushita's Megtron 5 also have significantly lower loss-tangent values at these higher frequencies (Nelco 6000-13SI is not available now). The loss-tangent value indicates a material degree of undesirable interaction with a signal at a given frequency.

Pc-board choices can be difficult to measure and a close relationship between laminate supplier and board fabricator is essential to achieve consistently high yield rates as well as acceptable long-term mean time between failures. There are many good materials but the best choice will be the one your vendor has already optimized from a processing perspective.

As has been done for AdvancedTCA, placing the hubs centrally for a VXS layout in most dual-star configurations is a good choice. Because of the superior loss-tangent characteristics, lower Er and other performance considerations, Bustronic chose a low-loss laminate for its 12-slot dual-star VXS prototype. For other future configurations that are less challenging (smaller slot counts, single-star configurations and so on) a standard FR-4 laminate may be sufficient.

Design challenges

To summarize the design challenges in general terms, three basic constraints will determine how the design engineer may achieve an interconnect design goal at these higher speeds. These constraints are length of the backplane path, the desired data rate and how many signals must be packed per inch of pc-board edge. The requirements for these three will drive the choice of semiconductor technology, pc-board materials, connectors, via construction and even other more-exotic constructions. Aside from the VITA and PICMG groups that are today implementing specific backplane architectures at 3.125 and 6.25 Gbits/s, there are study groups within the IEEE and the Optical Internetworking Forum that are addressing design matters for single-channel backplane interconnects capable of data rates up to 10 Gbits/s.

Regardless of the approach taken, the higher data rates in AdvancedTCA, VXS and other designs require creative backplane design solutions.

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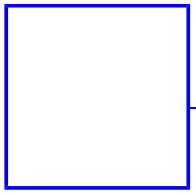

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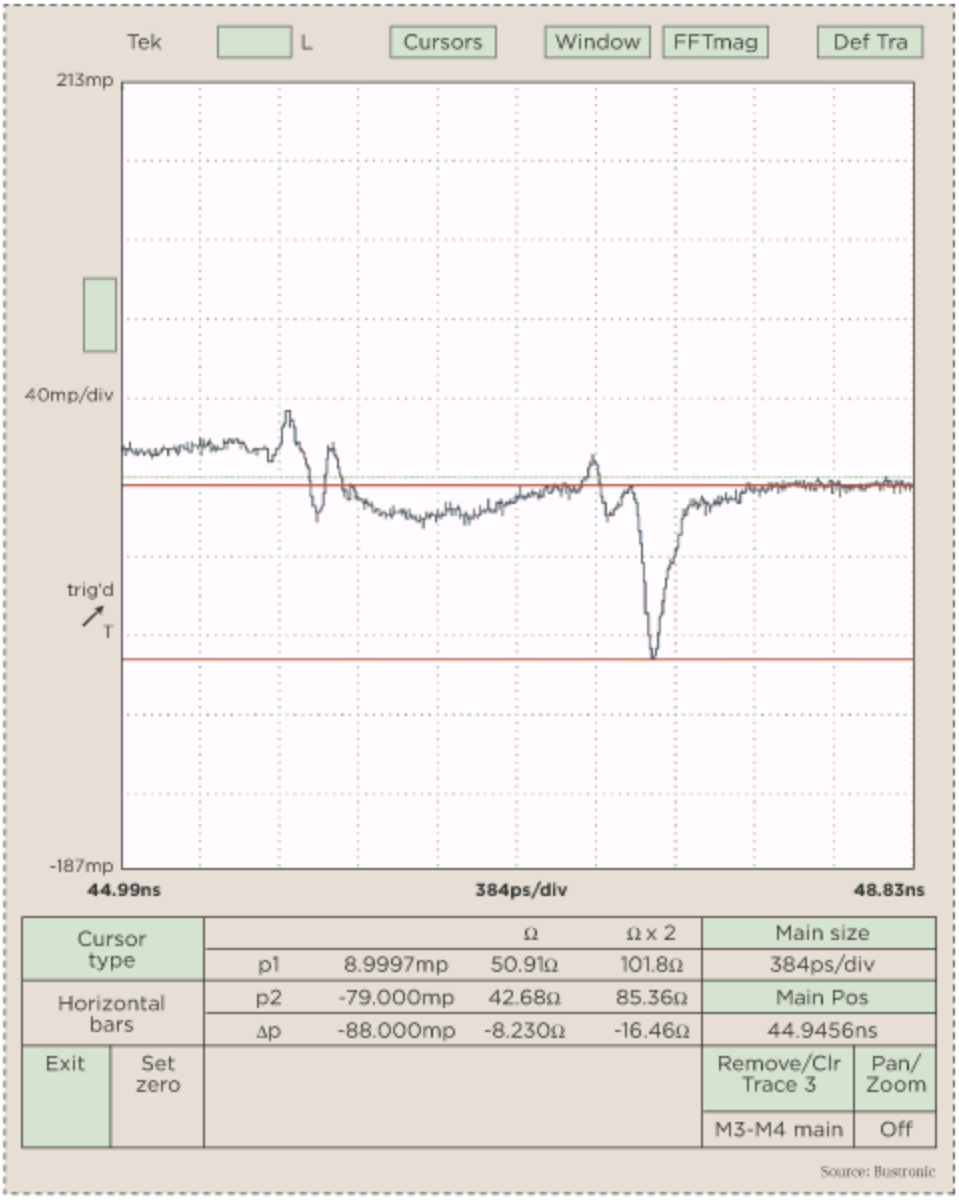

Time domain reflectomer profile of the first signal layer of an AdvancedTCA backplane shows a minimum differential impedance of just 85 ohms and backplane impedance of about 102 ohms. Stringent pc-board manufacturing yields the tight 2 percent tolerance.