System Management and Control Plane Partitioning Alternatives Facilitates System Flexibility

Until the development of the pin assignments proposed within VITA 41.7, there has been an apparent contact between VITA 41.6 an (GigE Control Plane) and the other VXS subsidiary documents with regards to the switch slot location already chosen for the terminus of the IPMI.

At first the problem appears to be another case of too many circuits in the space allocated. VITA 41.0 places the System Management Hub in the J1 connector of a fabric slot and VITA 41.6 saw no choice but to places the GigE control plane hub connections in the same location. This would have meant that users would have to choose between support for System Management and support for a separate control plane. For VXS applications that may hope to implement a system management controller in the future, this created an unfortunate situation.

However, in some cases the solution to a problem offers an improvement over the original design. It may be that the solution to the conflict over the use of the J1 connector position within VXS switch slots will offer an improvement to the VXS architecture overall. This white paper will show a creative solution which not only solves the basic dilemma but will explain why a solution that allows support for both a new control plane as well as system management is a good general solution for the VXS architecture. The arguments for the general adoption of this approach is based on the resulting system modularity which will ultimately reduce the number of necessary processor boards and VXS fabric switch cards that will be required for each board manufacturer and will also potentially free up valuable PCB area on VXS fabric cards.

The purpose of this white paper is to propose three alternate solutions that provide for:

a) A Fabric Switch with an integrated System Management hub controller.
b) A Fabric Switch with an integrated Control Plane hub switch.
c) Both Control plane hub and system management hub controllers located elsewhere in the system.

Background – How VITA 41.0 Is Currently Defined

Figure 1 below: VXS Payload J0 connector signals as currently assigned by VITA 41.0

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row I
1	PA_RX0+	PA_RX0-	GND	GND	PA_TX0+	PA_TX0-	GND	GND	PA SCL
2	GND	GND	PA_RX1+	PA_RX1-	GND	GND	PA_TX1+	PA_TX1-	GND
3	PA_RX2+	PA_RX2-	GND	GND	PA_TX2+	PA_TX2-	GND	GND	PA SDA
4	GND	GND	PA_RX3+	PA_RX3-	GND	GND	PA_TX3+	PA_TX3-	GND
5	RFU	RFU	GND	GND	RFU	RFU	GND	GND	RFU
6	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
7	RFU	RFU	GND	GND	RFU	RFU	GND	GND	RFU
8	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
9	RFU	RFU	GND	GND	RFU	RFU	GND	GND	RFU
10	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
11	RFU	RFU	GND	GND	RFU	RFU	GND	GND	PEN*
12	GND	GND	PB_RX0+	PB_RX0-	GND	GND	PB_TX0+	PB_TX0-	GND
13	PB_RX1+	PB_RX1-	GND	GND	PB_TX1+	PB_TX1-	GND	GND	PB SCL
14	GND	GND	PB_RX2+	PB_RX2-	GND	GND	PB_TX2+	PB_TX2-	GND
15	PB_RX3+	PB_RX3-	GND	GND	PB_TX3+	PB_TX3-	GND	GND	PB SDA

In figure 1 above, the original J0 signal assignments as they are currently designated within VITA 41.0 are shown. In Figure 2 below, are the J0 signal assignments as they are proposed within VITA 41.6. So far as the payload card J0 connector is concerned, this new solution adopts the proposal of VITA 41.6 (Control Plane on VXS) unchanged. This same proposed table of signal assignments will also be found as the recommended design for VITA 41.7 Processor Mesh on VXS.

Figure 2 below: Payload J0 with the two new control plane circuits, "PA_SG" and "PB_SG".

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row I
1	PA_RX0+	PA_RX0-	GND	GND	PA_TX0+	PA_TX0-	GND	GND	PA SCL
2	GND	GND	PA_RX1+	PA_RX1-	GND	GND	PA_TX1+	PA_TX1-	GND
3	PA_RX2+	PA_RX2-	GND	GND	PA_TX2+	PA_TX2-	GND	GND	PA SDA
4	GND	GND	PA_RX3+	PA_RX3-	GND	GND	PA_TX3+	PA_TX3-	GND
5	PA_SGRX+	PA_SGRX-	GND	GND	PA_SGTX+	PA_SGTX	GND	GND	RFU
6	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
7	RFU	RFU	GND	GND	RFU	RFU	GND	GND	RFU
8	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
9	RFU	RFU	GND	GND	RFU	RFU	GND	GND	RFU
10	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
11	PB_SGRX+	PB_SGRX-	GND	GND	PB_SGTX+	PB_SGTX	GND	GND	PEN*
12	GND	GND	PB_RX0+	PB_RX0-	GND	GND	PB_TX0+	PB_TX0-	GND
13	PB_RX1+	PB_RX1-	GND	GND	PB_TX1+	PB_TX1-	GND	GND	PB SCL
14	GND	GND	PB_RX2+	PB_RX2-	GND	GND	PB_TX2+	PB_TX2-	GND
15	PB_RX3+	PB_RX3-	GND	GND	PB_TX3+	PB_TX3-	GND	GND	PB SDA

Note that the System Management signals are shown in both Figure 1 and Figure 2. These are the lightly shaded PA_SCL/PA_SDA and PB_SCL/PA_SDA IPMB circuits in the upper and lower left hand corners of both chars. These signals have been part of VXS since the beginning and are there for the eventual implementation of System Management per VITA 38.

The new circuits shown in Figure 2 are shown in pink. These signals constitute PA_SG and PB_SG and are used to implement a VXS control plane that is being added as part of VITA 41.6. These have a value even in systems with or without system management and have been requested by board vendors who intend to use the control plane as a way to configure cards and initiate processes. Customers have resisted "splitting off" part of either of the two 10Gig center fabric channels for this purpose.

Figure 3 below: VXS Fabric switch slot J1 as currently assigned within VITA 41.0

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H
1	PEN*	RFU	SERA	SERB	+5 STBY	ACFAIL*	SYSFAIL8	SYSRST*
2	GA0*	GA1*	GA2*	GA3*	GA4*	GAP*	LI/I	RFU
3	SW SE1	SW SE2	SW SE3	SW SE4	SW SE5	SW SE6	SW SE7	SW SE8
4	SW TX+	SW TX-	SW RX+	SW RX-	RFU	RFU	RFU	RFU
5	PP5_SCL	PP3_SCL	PP1_SCL	PS1_SCL	PS2_SCL	PP2_SCL	PP4_SCL	PP6_SCL
6	PP5_SDA	PP3_SDA	PP1_SDA	PS1_SDA	PS2_SDA	PP2_SDA	PP4_SDA	PP6_SDA
7	PP11_SCL	PP9_SCL	PP7_SCL	PS1_ALRT	PS2_ALRT	PP8_SCL	PP10_SCL	PP12_SCL
8	PP11_SDA	PP9_SDA	PP7_SDA	PS1_SDA	PS2_SDA	PP8_SDA	PP10_SDA	PP12_SDA
9	PP18_SCL	PP15_SCL	PP13_SCL	PS3_SCL	PP4_SCL	PP14_SCL	PP16_SCL	PP18_SCL
10	PP17_SDA	PP15_SDA	PP13_SDA	PS3_ALRT	PP4_ALRT	PP14_SDA	PP16_SDA	PP18_SDA
11				DSP_SCA	DSP_SDA	DSP_ALRT		
12	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
13	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
14	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
15	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
16	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

The signals in dark blue and light blue are intended for the implementation of the System Management bus. However, there are not enough pins in the connector to accommodate the additional signals that would be required to also provide full support for a Control Plane Hub as defined in VITA 41.6.

So, VITA 41.6 currently proposes to eliminate the IPMB signals and simply re assign the J1/P1 connector to implement the hub for the control plane switch. For users and developers who expect to never require system management, this can be an adequate solution.

Figure 4 below: Fabric switch slot as currently proposed in VITA 41.6 VXS Control Plane.

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H
1	PEN*	RFU	SERA	SERB	+5 STBY	ACFAIL*	SYSFAIL8	SYSRST*
2	GA0*	GA1*	GA2*	GA3*	GA4*	GAP*	LI/I	RFU
3	SW SE1	SW SE2	SW SE3	SW SE4	SW SE5	SW SE6	SW SE7	SW SE8
4	SW TX+	SW TX-	SW RX+	SW RX-	RFU	RFU	RFU	RFU
5	GND	GND	GND	GND	GND	GND	GND	GND
6	PP17_SGTX+	PP17_SGTX-	PP15_SGTX+	PP15_SGTX-	PP17SGRX+	PP17_SGRX-	PP15_SGRX+	PP15_SGRX-
7	PP9_SGTX+	PP9_SGTX-	PP7_SGTX+	PP7_SGTX-	PP9_SGRX+	PP9_SGRX-	PP7_SGRX+	PP7_SGRX-
8	PP1_SGTX+	PP1_SGTX-	PP2_SGTX+	PP2_SGTX-	PP1SGRX+	PP1_SGRX-	PP2_SGRX+	PP2_SGRX-
9	PP8_SGTX+	PP8_SGTX-	PP10_SGTX+	PP10_SGTX-	PP8SGRX+	PP8_SGRX-	PP10_SGRX+	PP10_SGRX-
10	PP16_SGTX+	PP16_SGTX-	PP18_SGTX+	PP18_SGTX-	PP16SGRX+	PP16_SGRX-	PP18_SGRX+	PP18_SGRX-
11	PP13_SGTX+	PP13_SGTX-	PP11_SGTX+	PP11_SGTX-	PP13SGRX+	PP13_SGRX-	PP11_SGRX+	PP11_SGRX-
12	PP5_SGTX+	PP5_SGTX-	PP3_SGTX+	PP3_SGTX-	PP5SGRX+	PP5_SGRX-	PP3_SGRX+	PP3_SGRX-
13	PP4_SGTX+	PP4_SGTX-	PP6_SGTX+	PP6_SGTX-	PP4SGRX+	PP4_SGRX-	PP6_SGRX+	PP6_SGRX-
14	PP12_SGTX+	PP12_SGTX-	PP14_SGTX+	PP14_SGTX-	PP12SGRX+	PP12_SGRX-	PP14_SGRX+	PP14_SGRX-
15	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
16	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

Three Proposed Solutions – Modularity, Flexibility and Economy

There are, however, alternate solutions that provide for the support of the IPMB controller hub and the Control Plane hub switch that avoid the conflicts and congestion of circuits in the switch slot. Three possible alternate solutions can be summarized as follows:

1. Locate the IPMB hub in the switch slot.
2. Locate the Control Plane hub in the switch slot.
3. Locate neither of the two functions in the switch slot.

For the most robust systems with the greatest capability, there are a number of reasons to recommend solution three above. This is because there are many potential advantages that will derive from partitioning the system functions and locating these two "utility" networks elsewhere in the system. Doing so may add significant flexibility as well as reduce cost by limiting the number of potential "flavors" of switch fabric cards that will represent further savings in deployment, repair, inventory and cost of the switch cards themselves.

It is important to point establish from the beginning that the design of payload cards would remain the same regardless of the location of either utility hub. In addition, a backplane set up to support Control Plane Hubs or IPMB Hubs elsewhere would still be compatible with Fabric Switch cards designed to support either of the first two options listed. However, in the scenario where the hub functions are located elsewhere, any hub resource on a system fabric card would be redundant and remain idle.

Option 1: IPMB Hub in the Fabric Switch Slot

The solution represented by the J1/P1 signal assignments in figure 5 is intended for systems where the System Management Controller is located on the Switch Fabric cards. However, in row 16 of the connector in figure 5, two Control Plane circuits are provided so that the Switch fabric card can be a node on the control plane network and can be addressed through a Control Plane Switch which is located elsewhere in the system. The Control Plane network is a separate channel that can be used to reprogram resources on any VXS card such as firmware or even FPGA configurations. The Control Plane network could also be used to initiate processes or to end processes serving as a "back door" onto any card in the system.

Figure 5 below: VXS Switch Slot J1 with Sys Mgmt Hub but with Ctrl Plane Switch elsewhere

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H
1	PEN*	RFU	SERA	SERB	+5 STBY	ACFAIL*	SYSFAIL8	SYSRST*
2	GA0*	GA1*	GA2*	GA3*	GA4*	GAP*	LI/I	RFU
3	SW SE1	SW SE2	SW SE3	SW SE4	SW SE5	SW SE6	SW SE7	SW SE8
4	SW TX+	SW TX-	SW RX+	SW RX-	RFU	RFU	RFU	RFU
5	PP5_SCL	PP3_SCL	PP1_SCL	PS1_SCL	PS2_SCL	PP2_SCL	PP4_SCL	PP6_SCL
6	PP5_SDA	PP3_SDA	PP1_SDA	PS1_SDA	PS2_SDA	PP2_SDA	PP4_SDA	PP6_SDA
7	PP11_SCL	PP9_SCL	PP7_SCL	PS1_ALRT	PS2_ALRT	PP8_SCL	PP10_SCL	PP12_SCL
8	PP11_SDA	PP9_SDA	PP7_SDA	PS1_SDA	PS2_SDA	PP8_SDA	PP10_SDA	PP12_SDA
9	PP18_SCL	PP15_SCL	PP13_SCL	PS3_SCL	PP4_SCL	PP14_SCL	PP16_SCL	PP18_SCL
10	PP17_SDA	PP15_SDA	PP13_SDA	PS3_ALRT	PP4_ALRT	PP14_SDA	PP16_SDA	PP18_SDA
11	RFU	RFU	RFU	DSP_SCA	DSP_SDA	DSP_ALRT	RFU	RFU
12	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
13	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
14	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
15	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
16	PB_SGRX+	PB_SGRX-	PA_SGRX+	PA_SGRX-	PB_SGTX+	PB_SGTX-	PA_SGTX+	PA_SGTX-

Option 2: Control Plane Hub in the Fabric Switch Slot

The solution represented by the J1/P1 signal assignments in figure 6 is intended for systems where the Control Plane switch is located on the Switch Fabric cards. In addition the four IPMB signals (in light blue) are added so that this card can participate as a node on a system management bus. Because it is possible to implement a bused System Management Controller, the three DSP signals (in light blue-green) are provided. A bussed System Management architecture would not be as robust as a radial system but because there would be two controllers, there would be full redundancy if one of the IPMB busses hung for some reason.

In this example when the Gigabit Ethernet control channel hub located in the switch slot, the switch slot still may be provisioned as a node on the IPMB system management bus (in turquoise). This is important because although the switch card is supporting the Gigabit Ethernet control plane hub, it still may be important that it can report its health to the system management controller that is located elsewhere in the system.

Figure 6 below: VXS Switch Slot with J1 Control Plane Hub and bussed Sys Mgmt Controller

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H
1	PEN*	RFU	SERA	SERB	+5 STBY	ACFAIL*	SYSFAIL8	SYSRST*
2	GA0*	GA1*	GA2*	GA3*	GA4*	GAP*	LI/I	DSP_ALRT
3	SW SE1	SW SE2	SW SE3	SW SE4	SW SE5	SW SE6	SW SE7	SW SE8
4	SW TX+	SW TX-	SW RX+	SW RX-	RFU	RFU	RFU	RFU
5	GND	GND	GND	GND	GND	GND	GND	GND
6	PP17_SGTX+	PP17_SGTX-	PP15_SGTX+	PP15_SGTX-	PP17SGRX+	PP17_SGRX-	PP15_SGRX+	PP15_SGRX-
7	PP9_SGTX+	PP9_SGTX-	PP7_SGTX+	PP7_SGTX-	PP9_SGRX+	PP9_SGRX-	PP7_SGRX+	PP7_SGRX-
8	PP1_SGTX+	PP1_SGTX-	PP2_SGTX+	PP2_SGTX-	PP1SGRX+	PP1_SGRX-	PP2_SGRX+	PP2_SGRX-
9	PP8_SGTX+	PP8_SGTX-	PP10_SGTX+	PP10_SGTX-	PP8SGRX+	PP8_SGRX-	PP10_SGRX+	PP10_SGRX-
10	PP16_SGTX+	PP16_SGTX-	PP18_SGTX+	PP18_SGTX-	PP16SGRX+	PP16_SGRX-	PP18_SGRX+	PP18_SGRX-
11	PP13_SGTX+	PP13_SGTX-	PP11_SGTX+	PP11_SGTX-	PP13SGRX+	PP13_SGRX-	PP11_SGRX+	PP11_SGRX-
12	PP5_SGTX+	PP5_SGTX-	PP3_SGTX+	PP3_SGTX-	PP5SGRX+	PP5_SGRX-	PP3_SGRX+	PP3_SGRX-
13	PP4_SGTX+	PP4_SGTX-	PP6_SGTX+	PP6_SGTX-	PP4SGRX+	PP4_SGRX-	PP6_SGRX+	PP6_SGRX-
14	PP12_SGTX+	PP12_SGTX-	PP14_SGTX+	PP14_SGTX-	PP12SGRX+	PP12_SGRX-	PP14_SGRX+	PP14_SGRX-
15	PB_SDA	PB_SCL	PA_SDA	PA_SDL	RFU	RFU	DSP_SDA	DSP_SCL
16	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

Option 3: Neither Hub in the Fabric Switch Slot

The solution represented by the J1/P1 signal assignments in figure 6 is intended for systems where neither the Control Plane switch nor the IPMB controller is located in the Fabric Switch slots. There are a number of reasons why this may be the preferred solution for the most demanding applications. However, as noted previously, this third solution will function as intended even if the Fabric Switch Cards chosen were designed and intended to be used for either of the other two solutions already explained.

Of course, in this case where hub support resources exist on the fabric switch card plugged into a slot conforming to figure 7, those resources will be idle. If however, these newly available RFU pins in the J1 connector have been used for custom signals that would be harmful to a switch card having an on-board shelf controller or control plane switch a keying method would have to be utilized to protect unintended card insertions. However, the capability to use a fabric switch card that has an on-board management controller, even though this function is actually being provided by a different system management controller, can be a significant advantage. This is because it will allow the system integrator the widest possible choice between all available fabric switch cards.

Figure 7 below: VXS Fabric Switch J1 with access to the control plane and to the IPMB bus (For systems with the Control Plane hub and System Management hum elsewhere**)**

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H
1	PEN*	RFU	SERA	SERB	+5 STBY	ACFAIL*	SYSFAIL8	SYSRST*
2	GA0*	GA1*	GA2*	GA3*	GA4*	GAP*	LI/I	DSP_ALRT
3	SW SE1	SW SE2	SW SE3	SW SE4	SW SE5	SW SE6	SW SE7	SW SE8
4	SW TX+	SW TX-	SW RX+	SW RX-	RFU	RFU	RFU	RFU
5	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
6	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
7	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
8	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
9	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
10	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
11	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
12	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
13	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
14	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
15	PB_SDA	PB_SCL	PA_SDA	PA_SDL	RFU	RFU	DSP_SDA	DSP_SCL
16	PB_SGRX+	PB_SGRX-	PA_SGRX+	PA_SGRX-	PB_SGTX+	PB_SGTX-	PA_SGTX+	PA_SGTX-

Mechanical Considerations for Option 3

For systems utilizing the signal assignments shown in figure 7 above, there is an important mechanical consideration. If system management controllers and control plane switch cards are going to be located elsewhere, the natural question is where. The possible answers to this question fall into two basic categories.

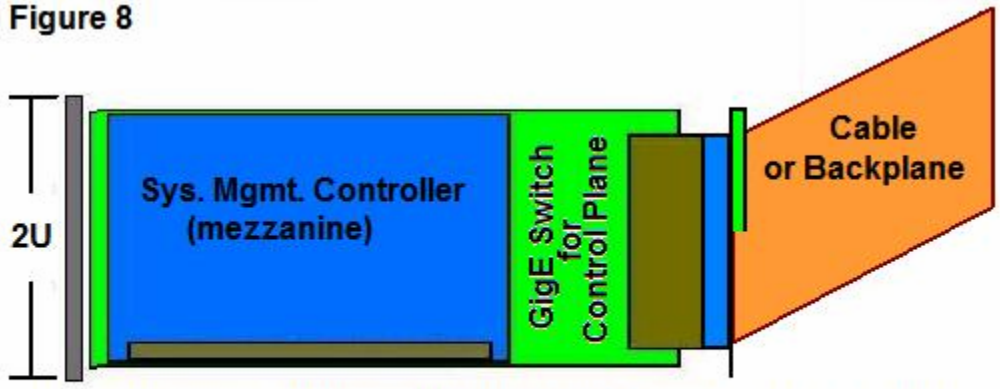
1. For smaller systems where cards are still arranged vertically but the entire width is not being utilized, plug in cards containing a Control Plane switch or a system management controller could be plugged into special slots. These cards do not need to be nearly as large as the other cards in the system so as many as three or four could be located in a single slot. Various arrangements are possible that will only be touched on briefly in this paper.
2. For larger systems where all the available card slots need to be reserved for various payload cards the plug in cards can be located in other areas of the system enclosure such “dead” regions of air plenums or in utility areas adjacent to power supplies. In this sort of topology, the control plane switch and the system management controller can be supported by separate backplanes or free connectors that are connected to the main VXS backplane via cable. This is already one solution being used in other architectures such as aTCA and PICMG 2.16. This is an extremely flexible solution. Another solution may be less expensive to service and deploy is to design a larger backplane that extends into a fan plenum or power supply area and provide the slots for these cards in the areas mentioned. This avoids the use of cables but requires a custom backplane.

System Management and Control Plane

Figure 8 below illustrates a plug in card that could serve both as a GigE switch for the Control Plane hub as well as contain a system management controller on a mezzanine. Two of these cards would support full redundancy.

Such cards could be stacked in a single slot as described in scenario 1 above. The same card could alternatively be connected by a ribbon cable to a rear socket on the main backplane. This solution would all full integration flexibility by allowing the card to be mounted in any available location.

Figure 8

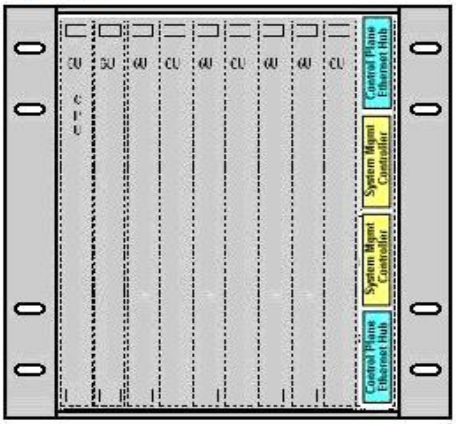


The GigE Control Plane Switch and the Sys. Mgmt. Controller could be combined on a single card. Such a card could plug directly into a backplane or could be connected by cable.

Figures 9 and 10 below show a front view of the two integration schemes described above.

In figure 9 the card(s) supporting the control plane switch or the system management controller could be stacked in an end slot. This would be convenient when the number of VXS and VME cards in the system do not occupy an entire subrack.

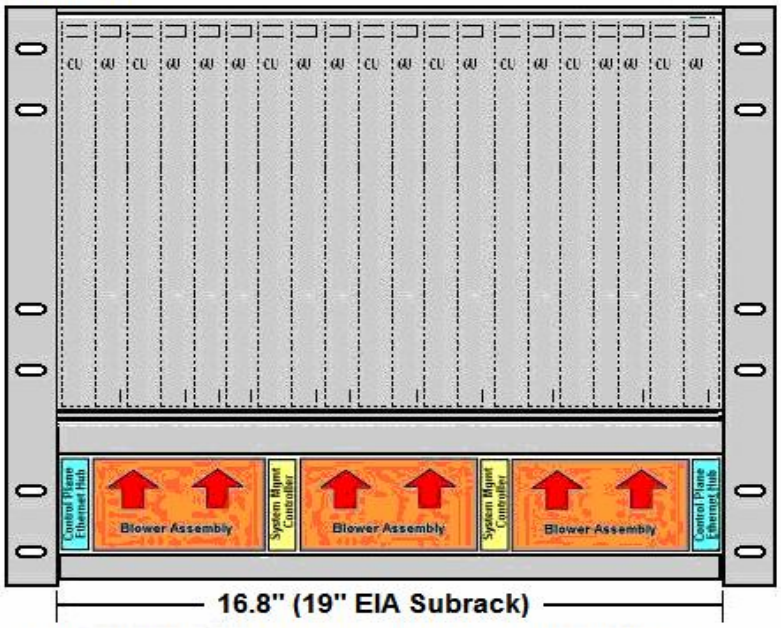
Figure 9



In smaller systems, the system management controller may be combined on a 3U plug in card with a GigE control plane switch.

Or they could be 4 separate cards also stacked.

Figure 10



This configuration can be supported by a custom backplane or the hub switch and management controller cards can be supported by cables to the main backplane.

For larger systems where every possible subrack slot needs to be preserved for system cards, then the utility controller/switch card(s) can be located in other available spaces. In other architectures, three large blowers offer four mounting slots for narrow cards that would not adversely effect the air flow, assuming an adequate mixing plenum.

COMPATIBILITY OF ALL THREE TOPOLOGIES

A backplane built with switch slot signal assignments in accordance with option three above as described by the table of signals in figure 7 can accept fabric cards that are wired for any of the three options (figures 5, 6 or 7), assuming that the RFU pins in P1 are not used.

However, there may be cases where a fabric card designed in accordance with figure 5 might be intentionally or unintentionally plugged into a backplane slot wired in accordance with figure 6 or vice versus. In these cases there is the likelihood of damage to the daughter card or the backplane or both. In addition, backplanes may be developed utilize the RFU pins indicated in figure 7 for some special application. In this case the same sort of incompatible and equipment damage could be expected.

It is necessary therefore to provide a unique keying scheme so that backplanes wired per figure 5 only accept similarly equipped daughter cards and likewise, for backplane slots wired per figure 6. Backplanes wired per figure 7 can accept any card; however, for custom implementations based on figure 7 wiring, a unique key would be required.

Fortunately, VXS provides for two key/guide locations in each fabric switch slot. Each of these two locations A1 and A2 also have both a keyed guide pins as well as an IEC socket for color coded plastic keys as used for the 2mm HM connector system. Figure 11 below, indicates in the yellow box a proposed guide position that would indicate. The other key values that have been defined thus far within VITA 41 and the subsidiary dot specs are also shown.

Figure 11 below: Guide Pin Values that have been thus far specified within the VXS subsidiary standards.

Angle	Key Value	Payload Card Slot Guide Position A0	Switch Card Slot Guide Position A1	Switch Card Slot Guide Position A2
0	1	Payload Standard	VXS Switch PWR Standard	No User IO on Switch
45	2			
90	3			
135	4			
180	5			
225	6			
270	7			No Ctrl Plane Switch No Sys Mgmt Hub
315	8			

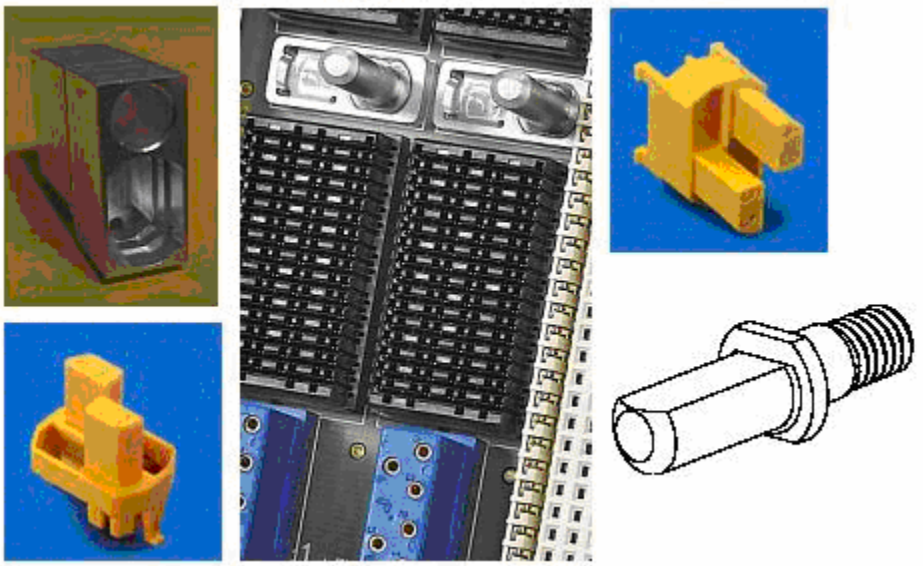
The IEC has defined 70 unique, color coded keys for the IEC sockets that are provided for the A0, A1 and A2 positions within VITA 41. There are ten of these plastic keys that are readily available without special ordering. The key assignments in the yellow boxes below define three

color keys for the position K2 to indicate the type of hub or switch that is supported by the switch slot.

Figure 12 below: Coding key designations that have been defined thus far within VITA 41 VXS standards.

B/P Key	D/C Key	Color	RAL	Payload Card Slot Key Position K0	Switch Card Slot Key Position K1	Switch Card Slot Key Position K2
1236	4578	Nut Brown	8011			J1 Ctrl Plane switch
1248	3567	Strawberry Red	3018			J1 Sys Mgmt hub
1356	2478	Blue Lilac	4005	IEEE 802.3 1000BASE T	IEEE 802.3 1000BASE T	
1567	2348	Brilliant Blue	5006	Infiniband 4x Links	Infiniband 4x Links	
2578	1346	Reseda Green	6011	PCI Express 4x Links	PCI Express 4x Links	No user IO connector
3456	1278	Cadmium Yellow	1021			No J1 Ctrl Switch No Sys Mgmt. hub
3467	1258	Slate Grey	7015			
3478	1256	Steel Blue	5011			
3568	1247	Pale Orange	2003	Serial Rapid IO	Serial Rapid IO	
4678	1235	Ocher Yellow	1024			

Figure 13 below: A graphic showing images of the backplane and daughter card coding keys sockets and guide pins used within the VXS family of standards (VITA 41.x).



List of Advantages for Option 3

Option 3 is the solution which this author proposes for all general VXS applications. This solution when implemented in the backplane, does not render any existing card inoperable, however, the adoption of option 3 for all backplanes would in the case of any existing VXS switch cards which are providing support for system management, require the addition of a redundant system management resource.

In addition to the obvious advantage of permitting the simultaneous support of both redundant system management controllers as well as dual GigE control plane switches, the partitioning of systems as described in option three (3) will have a number of other significant advantages.

Advantage 1 - The switch slots are already being crammed with FPGAs compute silicon as well as the various flavors of 10Gbs central fabric switching so space is at a premium.

Advantage 2 - Not all customers will need system management and those who do, if they were to implement Processor Mesh would certainly not need system management on all the switch blades. Separating the functions will allow greater flexibility.

Advantage 3 - The GigE control fabric will always be Ethernet but the switch cards are fabric specific to each architecture. So, separate Control Fabric switches and system controllers could be used across all systems instead of being integrated into a variety of other flavor switch cards. Also, you could support different system control features without forcing this variation on the main switch cards.

Advantage 4 - You can deploy a system enclosure with only a single shelf manager and one Control Fabric switch. The chassis can be on standby empty except for those two boards yet; you can manage it remotely, monitor its environmental readings without the expense of function cards and without the risk that this backup unit will have function cards that eventually are out of date and need to be updated before the chassis was ever called into service.

Advantage 5 - Different functions may be best supplied by different board vendors. An integrator can also use their own system management scheme but still have the option of going to an outside source for the fabric switch or processor blades.